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	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER	6
APPLICATION NO 	٠.	365-251	1315	2818	III TU	HO

Leonard Forbes Jerome Eldridge Kie Ahn

Programmable array logic or memory devices with asymmetrical tunnel barriers

ISSUING CLASSIFICATION						
ORIGINAL		CROSS REFERENCE(S)				
CLASS SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
157 / 314 /	257	315 239				
INTERNATIONAL CLASSIFICATION						
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		Continued on Issue Slip Inside File Jacket				

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED		
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.	
☐ The term of this patent	77 77 110 201		NOTICE OF ALL	OWANCE MAILED		
subsequent to	TLE-TUE HO: 02/04 (Assistant Examiner) (Date)		2-13-	04		
of U.S Patent. No.	David Nelms			ISSUE FEE		
	Supervisory Patent Examiner		Amount Due	Date Paid		
		hnology Center 2	2800 2 / Or (Date)	\$ 1630		
The terminalmonths of this patent have been disclaimed.	S Ma Klagal Instrument	Let (	7-17-04 (Date)	ISSUE BAT	CH NUMBER	
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The information disclosed herein may be rest Possession outside the U.S. Patent & Traden	tricted. Unauthorized nark Office is restricte	disclosure may be d to authorized emp	prohibited by the ployees and contra	United States Code Title 35, ctors only.	Sections 122, 181 and 368	

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